400G QSFP-DD FR4 Optical Transceiver

Product Features

- Compliant with 100G Lambda MSA 400G-FR4 specification
- Hot-pluggable QSFP-DD form factor
- Duplex LC connector
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Up to 106.25Gbps (PAM4) per channel
- 4 CWDM lanes MUX/DEMUX design
- Up to 2km link length over G.652 fiber with FEC
- Single +3.3V power supply
- Maximum power dissipation:12W
- Operation case temperature: 0 to 70°C
- RoHS compliant

Application

- Data Center Interconnect
- 400g Ethernet
- InfiniBand Interconnect
- Enterprise Networking

Absolute Maximum Ratings

Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	°C	-40		85	
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Power Supply not Damaged Voltage	V	-0.5		3.6	
Damaged Input Optical Power, Each Lane	dBm	4.5			

Recommended Operating Conditions

Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	°C	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		26.5625		
Pre-FEC Bit Error Ratio				2.4E-4	
Post-FEC Bit Error Ratio				1E-12	1
Link Distance	D	0.002		2km	2

1. FEC is provided by host system.
2. FEC is required on host system to support maximum distance.

Optical Characteristics

The following optical characteristics are defined over the recommended operating environment unlessotherwise specified.

Parameter	Unit	Min.	Typical	Max.	Note
Transmitter					
Signaling rate, each lane	GBd	53.125 ± 100 ppm			
Modulation format		PAM4			
Lane wavelengths (range)	nm	1264.5	1271	1277.5	
	nm	1284.5	1291	1297.5	
	nm	1304.5	1311	1317.5	
	nm	1324.5	1331	1337.5	
Side-mode suppression ratio (SMSR)	dB	30			
Total average launch power	dBm			9.3	
Average launch power, each lane	dBm	-3.3		3.5	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	dBm	-0.3		3.7	2
Difference in launch power between any two lanes (OMA_{outer})	dB			4	
Launch power in OMA_{outer} minus TDECQ, each lane (min): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	dBm	 -1.7 -1.6			
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	dB			3.4	
TDECQ–10*$\log_{10}(C_{eq})$, each lane	dB			3.4	3
Extinction ratio, each lane	dB	3.5			
$RIN_{17.1}OMA$	dB/Hz			-136	
Optical return loss tolerance	dB			17.1	
Transmitter reflectance	dB			-26	
Transmitter transition time	ps			17	
Average launch power of OFF transmitter, each lane	dBm			-20	
Receiver					
Data rate, each lane	GBd	53.125 ± 100 ppm			
Modulation format		PAM4			
Damage threshold, each lane	dBm	4.5			4
Average receive power, each lane	dBm	-7.3		3.5	5
Receive power (OMA_{outer}), each lane	dBm			3.7	

Difference in receive power between any two lanes (OMA_{outer})	dB			4.1	
Receiver sensitivity (OMA_{outer}), each lane (max)	dBm			Equation(1)	6
Stressed Receiver Sensitivity (OMA_{outer}), each lane	dBm			-2.6	7
Receiver Reflectance				-26	
LOS Assert	dBm	-20			
LOS De-Assert	dBm			-10.3	
LOS Hysteresis	dB	0.5			
Conditions of stressed receiver sensitivity test (Note 8)					
Stressed eye closure for PAM4 (SECQ), lane undertest	dB		3.4		
OMA_{outer} of each aggressor lane	dBm		1.5		
SECQ – 10*log10(Ceq), lane under test	dB			3.4	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratioof < 4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for referenceequalizer noise enhancement.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 1.

$$RS = \max(-4.6, SECQ - 6.0)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

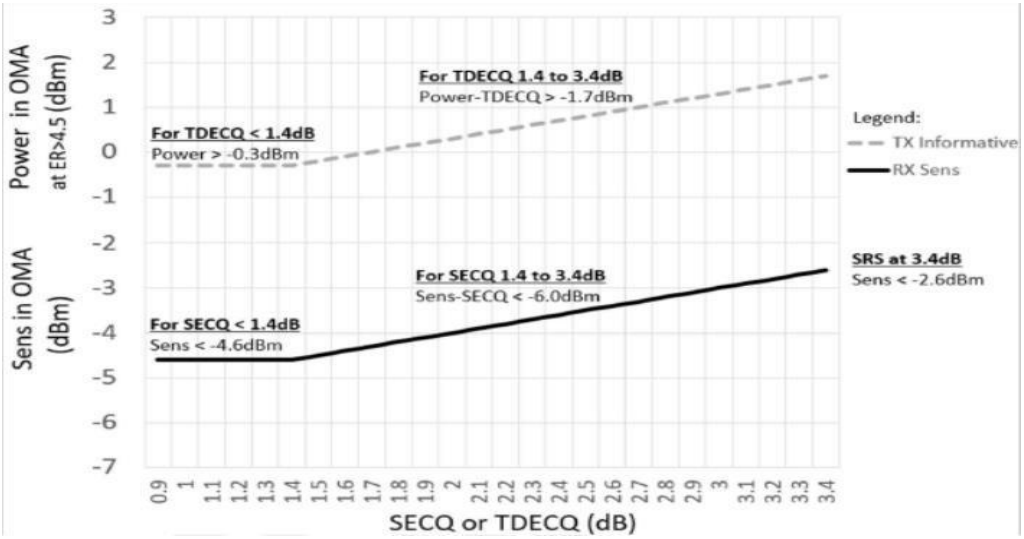

Figure 1. Illustration of Receiver Sensitivity Mask for 400G-FDR4

7. Measured with conformance with test signal at TP3 for the BER equal to 2.4E-4.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of thereceiver.

Electrical Specifications

The following electrical characteristics are defined over the Recommended Operating Environment unlessotherwise specified.

Parameter	Unit	Min.	Typical	Max.	Notes
Power consumption	W			12	
Supply current	A			3.64	
Transmitter (each lane)					
Signaling rate, each lane	GBd	26.5625 ± 100 ppm			
Differential pk-pk input voltage tolerance	mVpp	900			1
Differential termination mismatch				10%	
Differential input return loss	dB	IEEE802.3-2015 Equation (83E-5)			
Differential to common mode input return loss	dB	IEEE 802.3-2015 Equation (83E-6)			
Module stressed input test		See IEEE 802.3bs 120E.3.4.1			2
Single-ended voltage tolerance range (min)	V	-0.4 to 3.3			
DC Common mode input voltage	mV	-350		2850	3

Receiver (each lane)					
Signaling rate, each lane	GBd	26.5625 ± 100 ppm			
Differential peak to peak output voltage	mVpp			900	
AC Common mode output voltage, RMS	mV			17.5	
Differential termination mismatch	%			10	
Differential output return loss		IEEE 802.3-2015 Equation (83E-2)			
Common to differential mode conversionreturn loss		IEEE 802.3-2015 Equation (83E-3)			
Transition time, 20%~80%	ps	9.5			
Near-end eye symmetry mask width (ESMW)	UI		0.265		
Near-end eye height, Differential	mV	70			
Far-end eye symmetry mask width (ESMW)	UI		0.2		
Far-end eye height, Differential	mV	30			
Far-end Pre-cursor ISI ratio	%	-4.5		2.5	
Common mode output voltage (Vcm)	mV	-350		2850	

Note:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unlessotherwise specified.

Parameter	Units	Error	Notes
Temperature Monitor	°C	±3	Over operating temperature range
Supply Voltage Monitor	V	±0.1	Over full operating range
RX Power Monitor	dB	±3	1
Bias Current Monitor	mA	±10%	
TX Power Monitor	dBm	±3	1

PIN Function Definitions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1

2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1

5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power Supply Transmitter	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note：

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within theQSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined forthe host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTxand VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on thehost. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contactwith additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Typical Interface Circuit

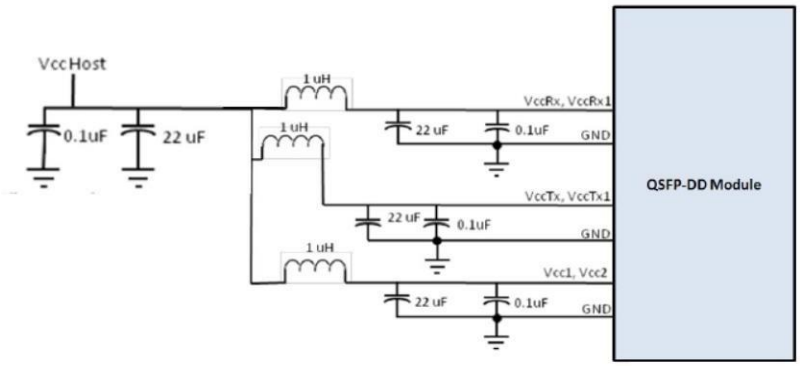

Figure 2. Recommended Power Supply Filter

Electrical Pad Layout

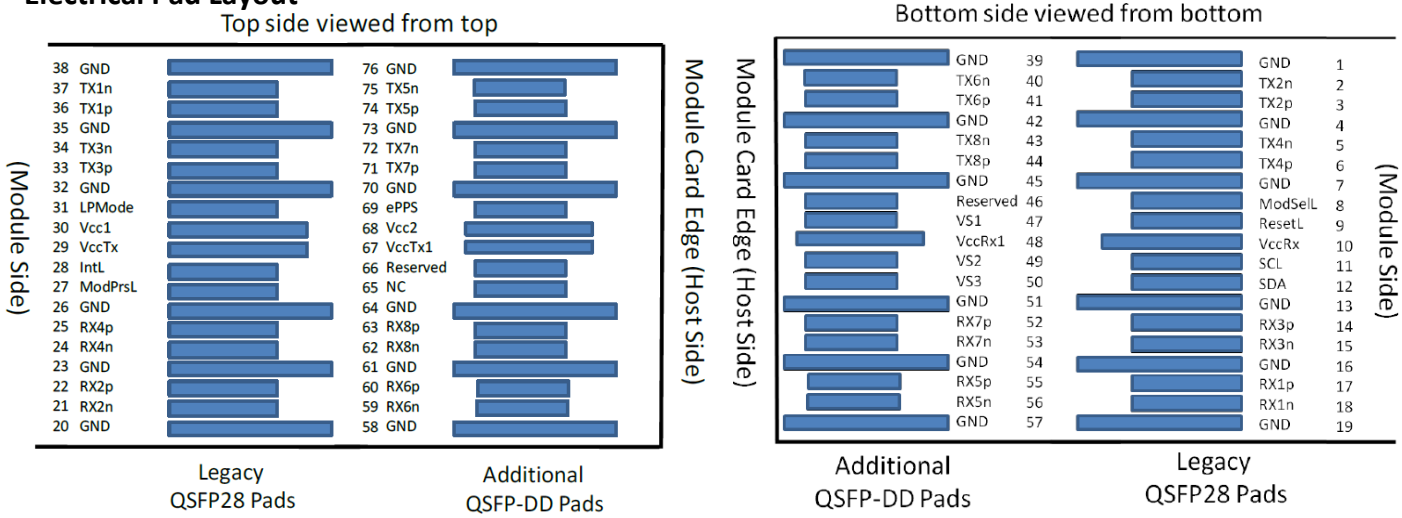

Figure 3：Module Pad Layout

Mechanical Specifications

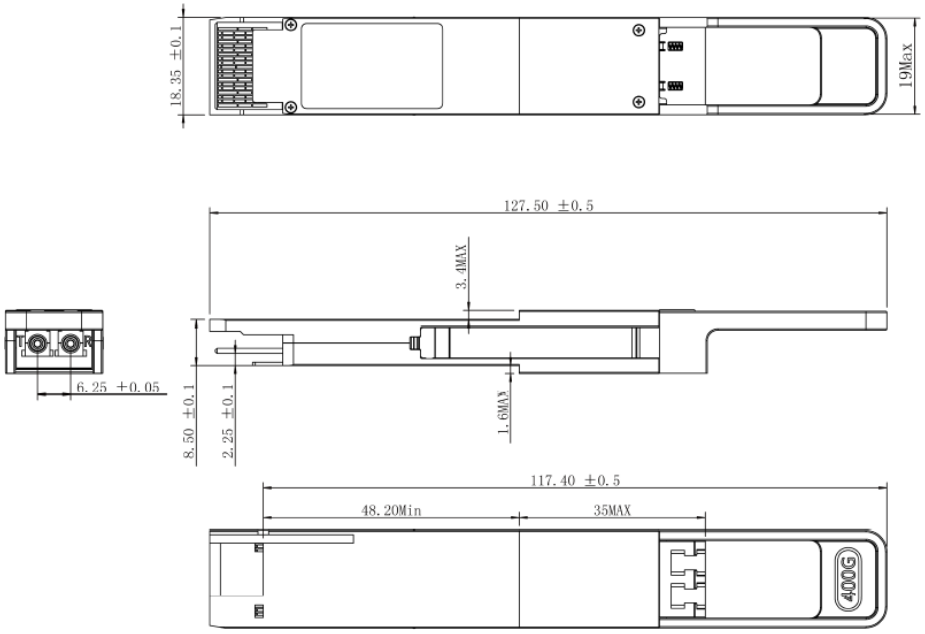

Figure 4. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Ordering Information

Ordering P/Ns	Description
QSFP-DD-FR4	2km, CWDM 1271/1291/1311/1331nm, 8*50G PAM4 electrical interface, 8*50G PAM4 at LC/UPC optical interface, QSFP-DD, commercial temperature