400Gbps QSFP-DD DR4

Optical Transceiver (Silicon Photonics)

Product Features

- Compliant with IEEE 802.3bs and QSFP-DD MSA
- Four parallel 1310nm optical lanes
- 8*53.125Gbps (PAM4) electrical interface (400GAUI-8),
- 4*106.25Gbps (PAM4) optical interface (1*12 APCMPO)
- Up to 500m transmission on single mode fiber (SMF) with FEC
- Maximum power consumption: 10W
- Operation case temperature: 0 to 70°C
- Compatible with QSFP-DD CMIS I2C Interface
- Compliant with RoHS requirement
- Laser safety class 1

Applications

- 400G Ethernet
- InfiniBand interconnects
- Data center and enterprise networking

Absolute Maximum Ratings

Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	°C	-40		85	
Operating Relative Humidity	%	0		85	
Power Supply Voltage	V	-0.5		3.63	
Damage Threshold	dBm	5			

Recommended Operating Conditions

Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	°C	0		70	
Power Supply Voltage	V	3.135	3.3	3.465	
Power Consumption	W			10	
Pre-FEC Bit Error Ratio			2.4E-4		
Post-FEC Bit Error Ratio			1E-12		1
Link Distance (DR4)	m	2		500	2
Link Distance (XDR4)	m	2		2000	2

Notes:

1. FEC is provided by host system.
2. FEC is required on host system to support maximum distance.

Electrical Characteristics

Parameter	Unit	Min.	Typical	Max.	Test point[1]	Notes
Transmitter						
Signaling Rate per lane (range)	GBd	26.5625 ± 100 ppm			TP1	
Differential pk-pk Input Voltage Tolerance	mVpp	900			TP1a	2
Differential Input Return Loss	dB	Equation (83E-5)			TP1	
Differential to Common Mode Input Return Loss	dB	Equation (83E-6)			TP1	
Differential Termination Mismatch	%			10	TP1	
Module Stressed Input Test		See 120E.3.4.1			TP1a	3
Single-ended Voltage Tolerance Range	V	-0.4		3.3	TP1a	
DC Common Mode Voltage	mV	-350		2850	TP1	4
Receiver						
Signaling Rate per lane(range)	GBd	26.5625 ± 100 ppm			TP4	
Peak-to-peak Differential Output Voltage	mVpp			900	TP4	
AC Common-Mode Output Voltage, RMS	mV			17.5	TP4	
Differential Output Return Loss		Equation (83E-2)			TP4	
Common to Differential Mode Conversion		Equation (83E-3)			TP4	
Differential Termination Mismatch	%			10	TP4	
Transition Time, 20% to 80%	ps	9.5			TP4	
Near-end ESMW (Eye Symmetry Mask Width)	UI		0.265		TP4	
Near-end Eye Height, Differential	mV	70			TP4	
Far-end ESMW (Eye Symmetry Mask Width)	UI		0.2		TP4	
Far-end Eye Height, Differential	mV	30			TP4	
Far-end Pre-cursor ISI Ratio	%	-4.5		2.5	TP4	
DC Common Mode Voltage	mV	-350		2850	TP4	4

Notes:

1. The location of TP1, TP1a and TP4 are defined in IEEE 802.3bs Figure 120E–5 and Figure 120E–6.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

All performance is defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Unit	Min.	Typical	Max.	Note
Transmitter					
Signaling Rate, per lane	GBd	53.125 ± 100 ppm			PAM4
TX Central Wavelength	nm	1304.5	1310	1317.5	
Side-mode Suppression Ratio (SMSR)	dB	30			
Average Launch Power, per lane	dBm	-2.9		4	1
Outer Optical Modulation Amplitude (OMA_{outer}), per lane	dBm	-0.8		4.2	2
Launch Power in OMA_{outer} minus TDECQ, each Lane	dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), per lane	dB			3.4	3
Average Launch Power of OFF Transmitter, per lane	dBm			-15	
Extinction Ratio, per lane	dB	3.5			
Optical Return Loss Tolerance	dB			21.4	
$RIN_{21.4}OMA$	dB/Hz			-136	
Transmitter Reflectance	dB			-26	
Receiver					
Signaling Rate, per lane	GBd	53.125 ± 100 ppm			PAM4
RX Central Wavelength	nm	1304.5	1310	1317.5	
Damage Threshold	dBm	5			4
Average Receive Power per Lane	dBm	-5.9		4.0	5
Receiving Power (OMA_{outer}) per Lane	dBm			4.2	
Receiver Reflectance (max)	dB			-26	
Receiver Sensitivity (OMA_{outer}), per lane(max)	dBm	Equation (1)			6
Stressed Receiver Sensitivity (OMA_{outer}), per Lane	dBm			-1.9	7
Conditions of Stressed Receiver Sensitivity Test:					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	dB		3.4		8
OMA_{outer} of each Aggressor Lane	dBm			4.2	
LOS Assert	dBm	-15			
LOS De-Assert	dBm			-8.9	
LOS Hysteresis	dB	0.5			

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
6. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation (1), which is illustrated in Figure 1.

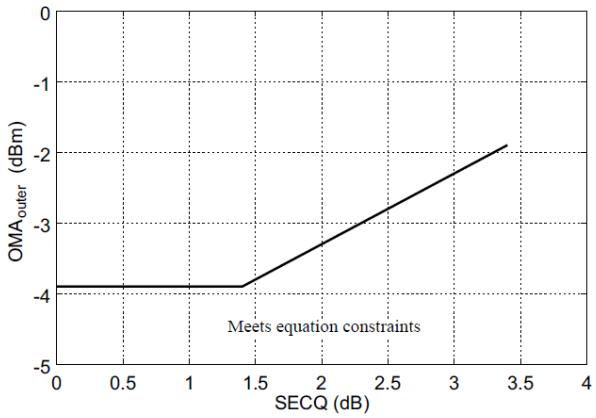


Figure 1. Illustration of Receiver Sensitivity Mask for 400G-DR4

$$RS = \max(-3.9, SECSS - 5.3)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver

Optical Interface

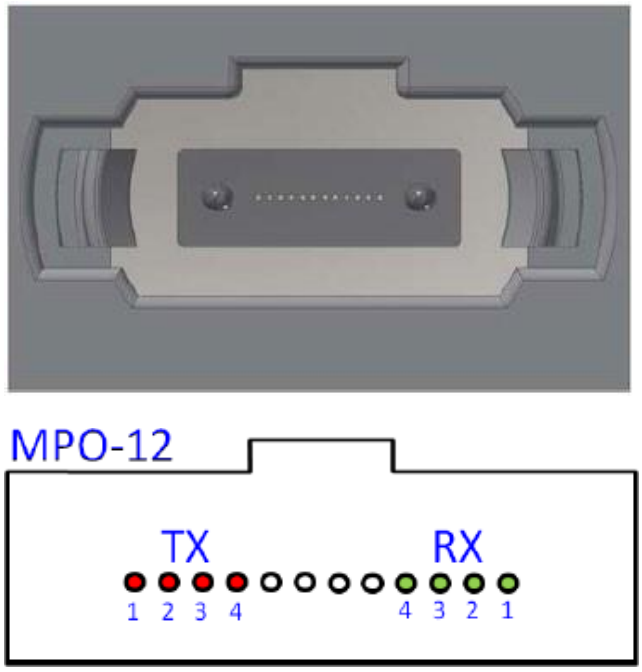
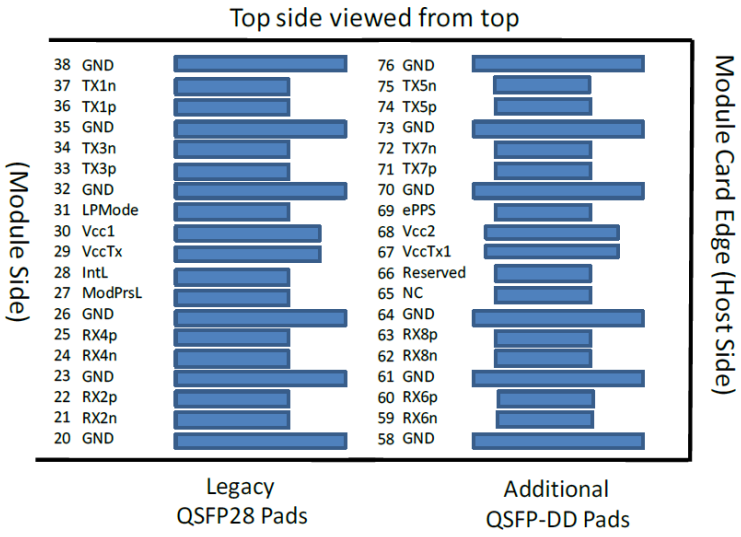


Figure 2: MPO-12 Single Row optical patch cord and module receptacle

Pin Assignment and Description



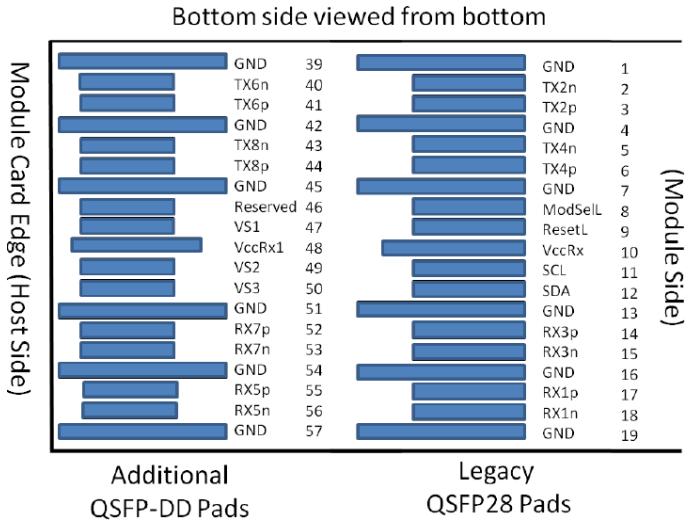


Figure 3：Module Pad Layout

PIN Function Definitions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	

22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power Supply Transmitter	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1

62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Recommended Power Supply Filter

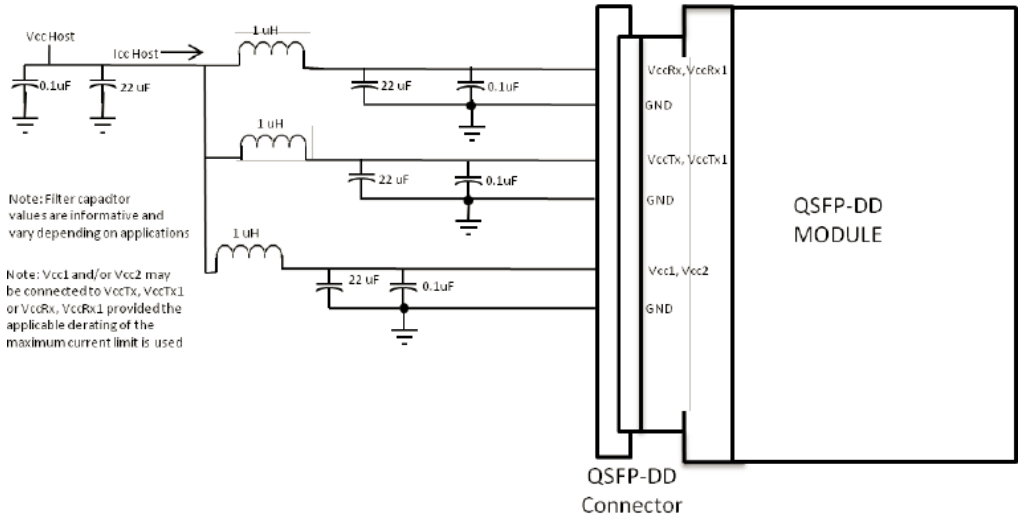


Figure 4: Recommended Host Board Power Supply Filtering

Mechanical Outlines

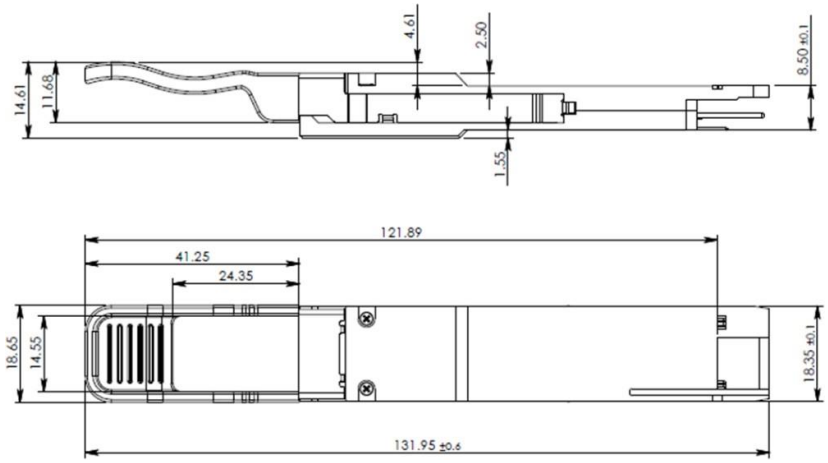
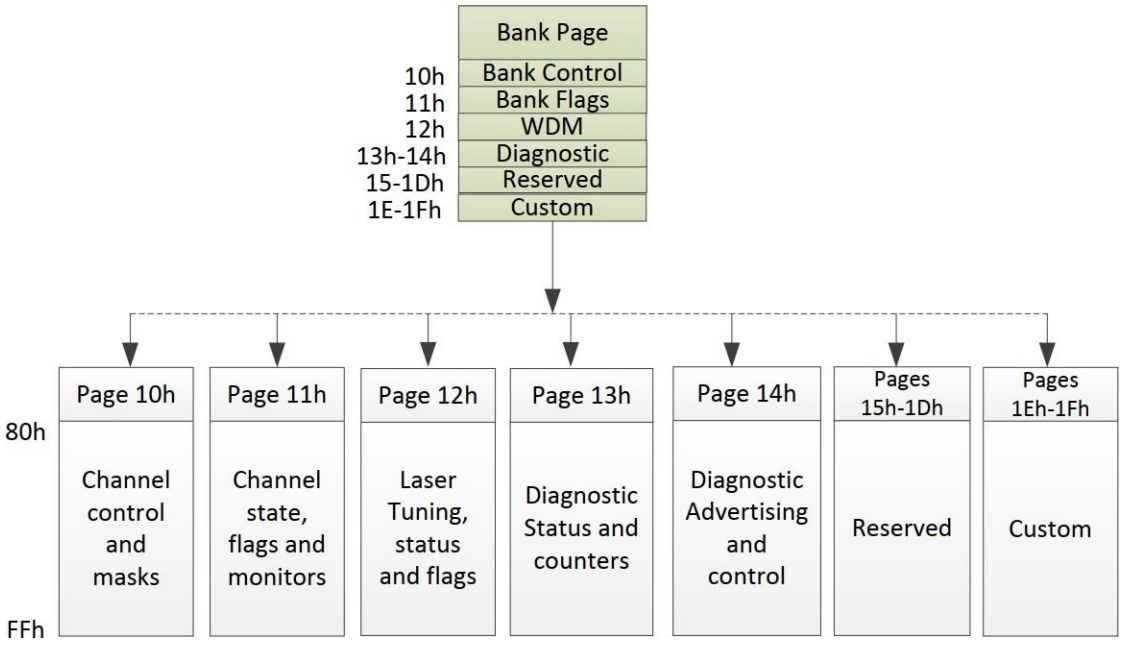


Figure 5. Mechanical Outline

Digital Diagnostic Functions

Parameter	Units	Error	NOTES
Temperature Monitor	°C	±3	1LSB=1/256°C
Supply Voltage Monitor	V	±0.1	1LSB=100uV
Bias Current Monitor	mA	±10%	1LSB=2uA
TX Power Monitor	dBm	±3	1LSB=0.1uW
RX Power Monitor	dBm	±3	1LSB=0.1uW



ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Ordering Information

Ordering P/Ns	Description
QSFP-DD-DR4	400G DR4, 1310nm 500m SMF, QSFP56-DD form-factor, 1*12 MPO APC receptacle, Commercial Temperature, Silicon Photonics based