100G QSFP28 10km Optical Transceiver Specification

Features

- QSFP28 Serial Optical Interface
  - Supports 103Gb/s data rate
  - 4*25G LAN-WDM cooled DML Lasers for up to 10km
  - 4 channels PIN detector
- QSFP28 MSA Compliant
  - Compliant with SFF-8679 for electrical interface
    - CAUI-4 High Speed electrical interface
  - Compliant with SFF-8661 for mechanical interface
    - QSFP28 Mechanical Interface for easy removal
    - Duplex LC Receptacle
  - Compliant with SFF-8636 for 2-wire interface for management and DDM
- Support Protocol
  - IEEE Std802.3ba
  - 100G Ethernet
- Low Power Consumption
  - Less than 4W in temperature range of 0 to 70℃

Applications

- 100G LR4 Ethernet links

1. General Description

L-QSFP28-LR4 transceiver modules are designed for 100Gigabit Ethernet over 10km single mode fiber. They are compliant with the 100GBASE-LR4 and IEEE 802.3ba. Each transceiver incorporates four direct modulated lasers with driver ICs, four PIN diodes with TIAs, and two Mux/De-Mux blocks in a highly integrated LAN-WDM configuration for operation over duplex LC connectors. Mechanical dimensions, connectors and the footprint of this product is QSFP28 specifications compliant. Digital Diagnostics functions are available via a 2-wire serial interface, as specified SFF-8636.

2. Absolute Maximum Ratings and Recommended Operating Conditions

Table 2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-40	85	degC
Relative Humidity (non-condensation)	RH	5	95	%
Supply Voltage	VccR/VccT	-0.5	3.6	V
Damage Threshold, each Lane	THd	5.5	-	dBm

Table 2.2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	0	70	degC
Relative Humidity(non-condensing)	Rhop	5	85	%
Power Supply Voltage	VccR/VccT	3.135	3.465	V
Power Supply Current	Irt	-	1212	mA
Total Power Consumption	Pc	-	4	W

3. Optical Specifications

3.1 Optical Transmitter

Table 3.1 Transmitter Optical Interface

Parameter		Symbol	Min	Typical	Max	Unit
Data rate per channel	100G Base LR4		25.78125+/100ppm			Gbps
Center Wavelength		L0	1294.53	1295.56	1296.59	nm
		L1	1299.02	1300.05	1301.09	nm
		L2	1303.54	1304.58	1305.63	nm
		L3	1308.09	1309.14	1310.19	nm
Side Mode Suppression Ratio		SMSR	30			dB
Total Average Launch Power		P_T			10.5	dBm
Average launch power, each Lane		P_{avg}	-4.3		4.5	dBm
OMA, each lane		P_{OMA}	-1.3		4.5	dBm
Transmitter and dispersion penalty		TDP			2.2	dB
Average launch power of Tx OFF		P_{ave_off}			-30	dBm
Extinction ratio		ER	4			dB
Spectral Width					1	nm
RIN OMA		RIN			-130	dB/Hz
Optical Return Loss Tolerance		ORLT			20	dB
Optical Power for TX DISABLE					-30	dBm
Transmitter Reflectance					-12	dB
Mask Margin			5			%

3.2 Optical Receiver

Table 3.2 Receiver Optical Interface

Parameter		Symbol	Min	Typical	Max	Unit
Data rate per channel	100G Base LR4			25.78125		Gbps
Center Wavelength		L0	1294.53	1295.56	1296.59	nm
		L1	1299.02	1300.05	1301.09	nm
		L2	1303.54	1304.58	1305.63	nm
		L3	1308.09	1309.14	1310.19	nm
Average receiver power，each lane[1]		P_{avg}	-10.6		4.5	dBm
Sensitivity	100G Base LR4, OMA per lane[2]				-8.6	dBm
Rx LOS	Assert		-24			dBm
	De-assert				-12.5	dBm
	Hysteresis		0.5			dB
Receiver Reflectance					-26	dB

Notes:

1. Minimum value is informative, equals min TxOMA with infinite ER and max channel insertion loss

2. Receiver sensitivity is measured with conformance test signal for BER=$1x10^{-12}$.

4. Electrical Specifications

Table 4.1 High Speed Electrical Specifications

Parameters	Min	Typical	Max	Unit
Signaling rate per lane		25.78125		Gbps
Supply voltage	3.135		3.465	V
Input differential impedance		100		Ω
Differential data input swing	150		900	mV
Differential data output swing	300		900	mV

Table 4.2 2-wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc voltage	Vcc_Host_2w	3.14	3.46	V
SCL and SDA Voltage[1]	V_{OL}	0.0	0.40	V
	V_{OH}	Vcc_Host_2w -0.5	Vcc_Host_2w +0.3	V
	V_{IL}	-0.3	VccT*0.3	V
	V_{IH}	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA contacts	I_I	-10	10	mA

Notes:

1. These voltages are measured on the other side of the connector to the device under test.

5. Timing Specifications

The module management interface is based on 2-wire interface. Management memory map is based on SFF-8636.

6. User Interface

6.1 Management Interface

2-Wire Serial Address: 1010000x（A0H）

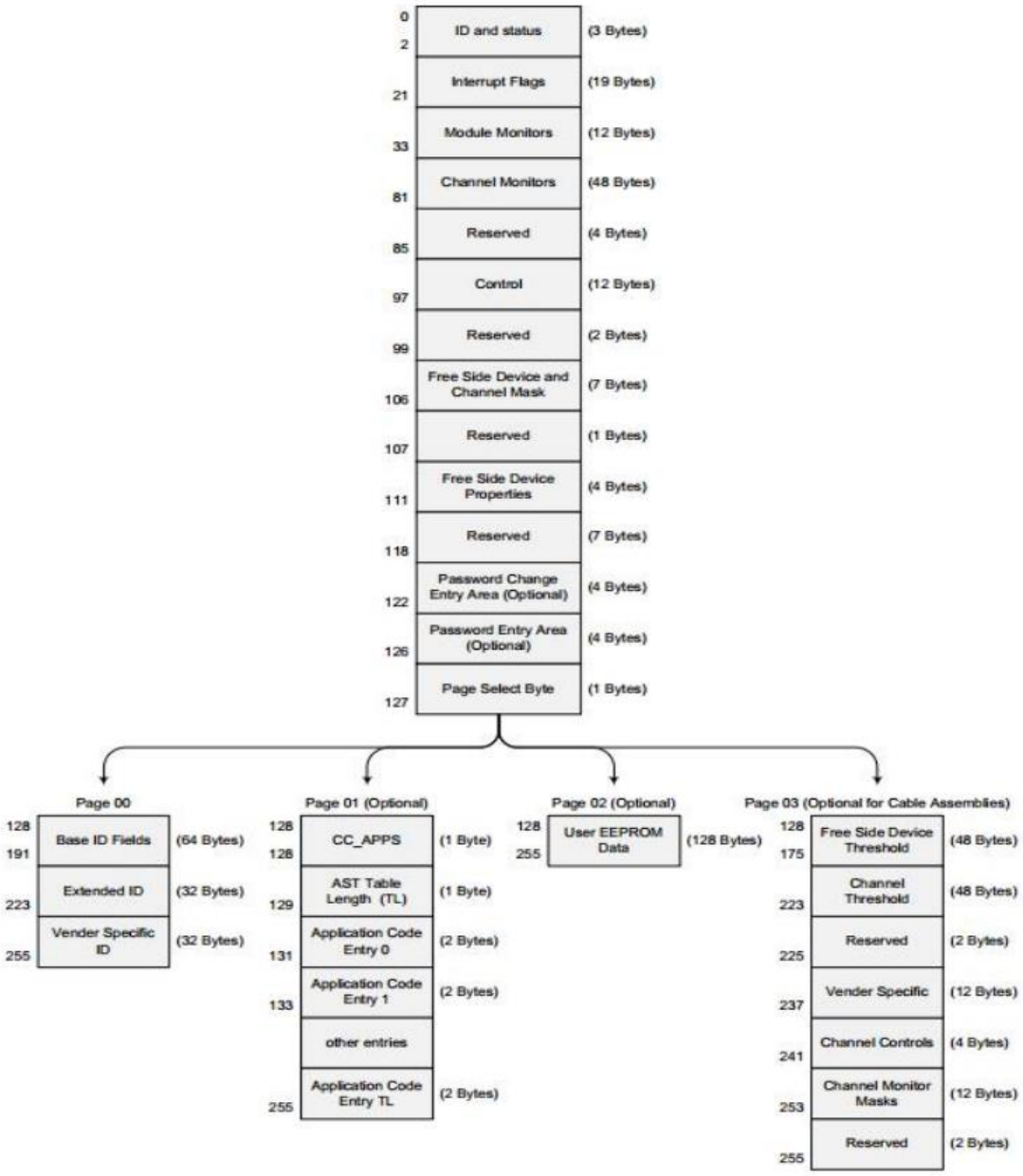

Figure 6.1 QSFP28 Memory Map

6.2 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Table 6.2 Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	±3	deg.C
Internally Measured Transceiver Supply Voltage	±3	%
Measured Tx Bias Current	±10	%
Measured Tx Output Power	±2	dB
Measured Rx Received Average Optical Power	±2	dB

7. Pin Assignment and Pin Description

7.1 PIN Definitions

QSFP28 transceiver pad layout, host PCB QSFP28 pinout, and PIN descriptions are as follows:

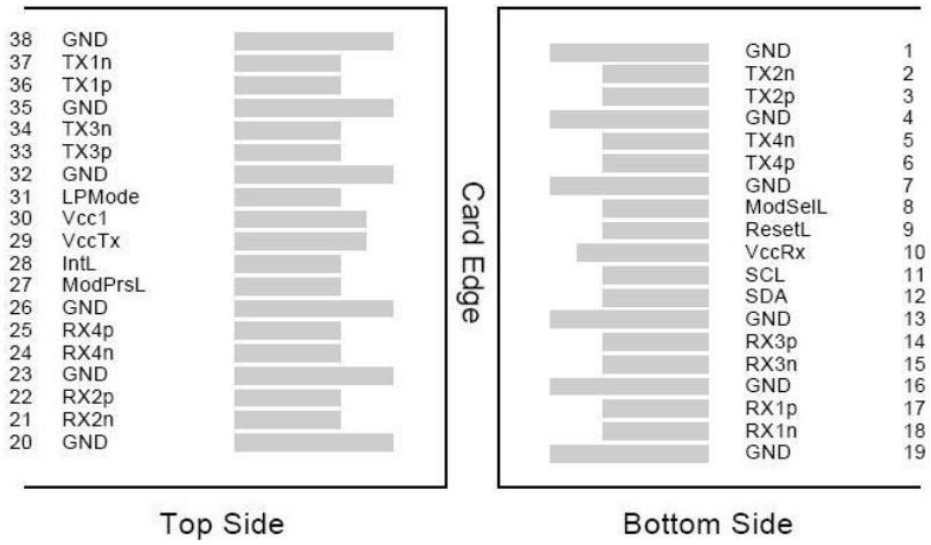

Figure 7.1 QSFP28 Transceiver Electrical Pad layout

7.2 PIN Description

Table 7.2 Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	3
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3	3
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	3
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	3
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note:

[1] GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

7.3 Multiplex LPMode and IntL

The LPMode PIN is multiplexed for TX_Disable and IntL PIN multiplexed for Rx_LOS according to customers' requirements

Table 7.3 Multiplex LPMode and IntL table

	LPMode	TX_Disable	IntL	RX_LOS
High	Asserted	Asserted	De-asserted	Asserted
Low	De-asserted	De-asserted	Asserted	De-asserted

Following MSA's design concept, when a new control feature is added, there should be two fields to define for the new feature, advertise (Read-Only) field to indicate if the feature is supported, and control field (R/W) to configure the new feature. In SFF8636, most of register in page 0 low are defined as R/W registers. Most register in page 0 high are defined as Read-Only registers.

Table 7.4 Definition of configuration register for Multiplex function

Registers	State	Description
Bit 0	0	IntL pin only. RX_LOS pin not supported.
	1	Both IntL and RX_LOS supported.
Bit 1	0	LPMode pin only. TX Disable not supported.
	1	Both LPMode and TX Disable supported

Table 7.5 Definition of control register for Multiplex function

Registers	State	Description
Bit 0	0	IntL pin active
	1 (Default)	RX_LOS active
Bit 1	0	LPMode pin active
	1 (Default)	TX Disable active

Note:

Register is read-only during high power mode and can only be modified at lower power mode.

8. Package Dimensions

Figure 8.1 shows the package dimensions of the module. The module is designed to be complaint with QSFP28 MSA specification. Package dimensions are specified in SFF-8661.

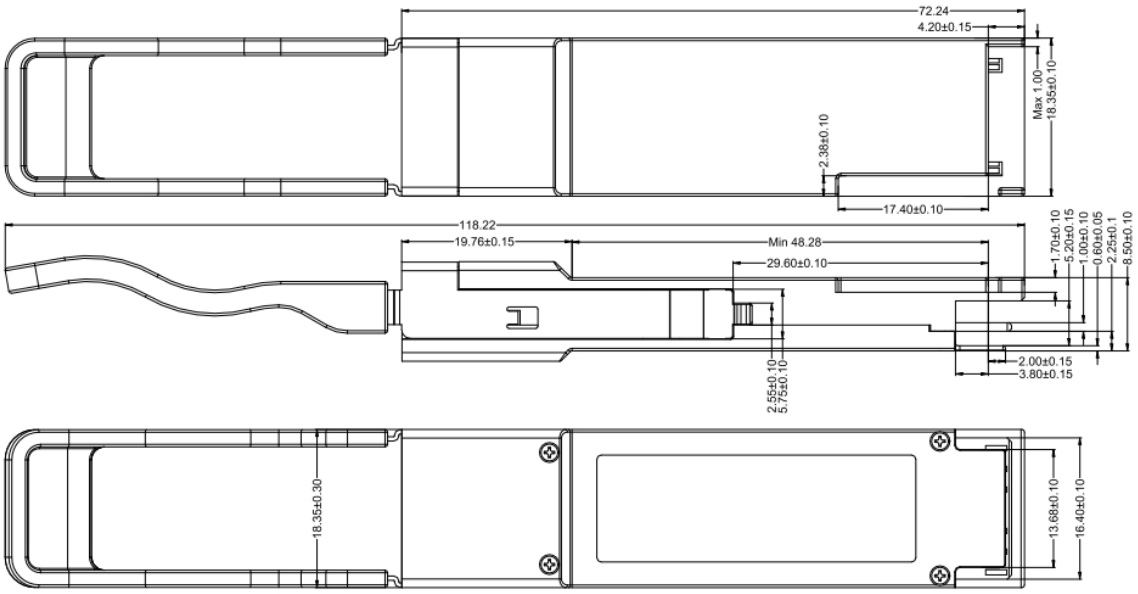

Figure 8.1 Package Dimensions

9. Laser safety and Electromagnetic Compatibility

9.1 Laser safety

All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825-1 & IEC60825-2 standards. They must be operated under specified operating conditions.

9.2 Electromagnetic Compatibility

All transceivers are designed to meet FCC Class B limits.

10. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E
L-QSFP-LR4-10	0˚C to + 70˚C	10km	SMF	DML	PIN