

50G QSFP28 40km ER Optical Transceiver Specification

Features

- 50 Gigabit Ethernet (50GbE) Transceiver
- Hot-pluggable QSFP28 form factor and Compliant with QSFP28 MSA
- Duplex LC connector
- Compliant to 26.5625 GBd/s PAM4 50GBASE-ER Optical Interface
- Compliant to 50GAUI-1 Serial Electrical Interface
- 2 x 26.5625Gb/s NRZ or 26.5625 GBd/s PAM4 electrical modulation
- Maximum link length of 40km on Single Mode Fiber (SMF)
- Optical Transmitter: 1310nm cooled EML
- Optical Receiver: APD photodetector with limiting amplifier
- Power Consumption < 4W
- I2C interface with integrated Digital Diagnostic Monitoring
- Operating Case Temperature: 0 to 70 °C
- Compliant to SFF-8636 and SFF-8679
- RoHS-6 complaint

Applications

50 Gigabit Ethernet (50GbE) Transceiver

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1. General Description

The L-QSFP-ER2-40 is a low power consumption QSFP28 PAM4 transceiver with high performance up to 50G high speed telecom and data communications over single mode fiber. It is compliant with the QSFP28 MSA, and IEEE 802.3cn. The Optical transmitter integrated with DSP that translated two lanes 26.5625Gb/s NRZ or one lane 26.5625GBd/s PAM4 to 26.5625GBd/s PAM4. It contains a single LC connector for the optical interface and a 38-pin connector for the electrical interface. Digital Diagnostics functions are available via a 2-wire serial interface, as specified SFF-8636.

2. Absolute Maximum Ratings and Recommended Operating Conditions

Table 2.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	85	$^{\circ}$
Storage Relative Humidity (non-condensation)		85	%
Supply Voltage	-0.5	3.6	V

Table 2.2 Recommended Operating Conditions

Parameter	Min	TYP.	Max	Unit
Operating Case Temperature	0		70	$^{\circ}$
Power Supply Voltage	3.135	3.3	3.465	V
Power Supply Current			1.2	А
Total Power Consumption			4	W
Data Rate(Optical) PAM4		26.5625		GBd/s
Data Rate(Electrical) NRZ		2x26.5625		Gb/s
Data Rate(Electrical) PAM4 (or)		26.5625		GBd/s
Transmission Distance			40	km

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3. Optical Specifications

3.1 Optical Transmitter

Table 3.1 Transmitter Optical Interface

Parameter	Min	Туре	Max	Unit	Note
Signaling Speed		26.5625		GBd/s	
Operating Wavelength Range	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	30			dB	
Average Launch Power	0.4		6.6	dBm	1
Optical modulation amplitude (OMAouter)	3.4		7.4	dBm	2
Extinction Ratio	6			dB	
Launch Power in OMAouter Minus TDECQ	2			dB	
Transmitter and dispersion eye closure for PAM4 (TDECQ)			3.2	dB	
RIN ₁₅ OMA			-132	dB/Hz	
Optical Return Loss Tolerance			15	dB	
Transmitter Reflectance			-26	dB	3

Notes:

[1]Min average power is informative and not the principal indicator of signal strength. Power below this value cannot be compliant; however, a value above this does not ensure compliance.

[2] Even if the TDECQ < 1 .4dB, the OMA outer (min) must exceed this value.

[3] Transmitter reflectance is defined looking into the transmitter.

3.2 Optical Receiver

Table 3.2 Receiver Optical Interface

Parameter	Min	Тур.	Max	Unit	Note
Signaling Speed		26.5625		GBd/s	
Wavelength Range	1304.5	1311	1317.5	nm	

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L-QSFP28-ER2-40

Damage Threshold	-2.4		dBm	1
Average Receive Power	-17.6	-3.4	dBm	2
Receiver Sensitivity (OMAouter)		Max(-15.1, SECQ – 16.5)	dBm	3
Stressed Receiver Sensitivity (OMAouter)		-13.3	dBm	4
Receiver Reflectance		-26	dB	
LOS Assert	-30		dBm	
LOS De-Assert		-20	dBm	
LOS Hysteresis	0.5		dB	

Notes:

- [1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
- [2] Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- [3] Receiver sensitivity (OMA outer) (max) is informative and is defined for a transmitter with a value of SECQ up to 3.2 dB for 50GBASE-ER. The value of BER is 2.4e-4 (before FEC).
- [4] Measured with conformance test signal at TP3 (see 139.7.10) for the BER specified in 139.1.1 (IEEE802.3cn)

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4. Electrical Specifications

Table 4.1 Transmitter (Module Input) Electrical Specifications

Parameters	Symbol	Min	Тур.	Max		Unit
Differential Data Input Amplitude	V _{IN,P-P}			900		mV
Differential Termination Mismatch				10		%
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3		0.8		V
LFINIOUE/TXDIS, Resett and Mouseit	VIH	2		VCC+0.3		V

Table 4.2 Receiver (Module Output) Electrical Specifications

Table 4.2 Neceiver (Module Output) Liectifical Specifications								
Parameters	Symbol	Min	Тур.	Max	Unit			
Differential Data Input Amplitude	Vout,p-p			900	mV			
Differential Termination Mismatch				10	%			
Output Rise/Fall Time, 20%~80%	TR	9.5			ps			
ModPrsL and IntL/RxLOSL	VIL	0		0.4	V			
IVIOUFISE AND INIL/RALUSE	VIH	VCC-0.5		VCC+0.3	V			

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5. User Interface

5.1 Management Interface

2-Wire Serial Address: 1010000x (A0H)

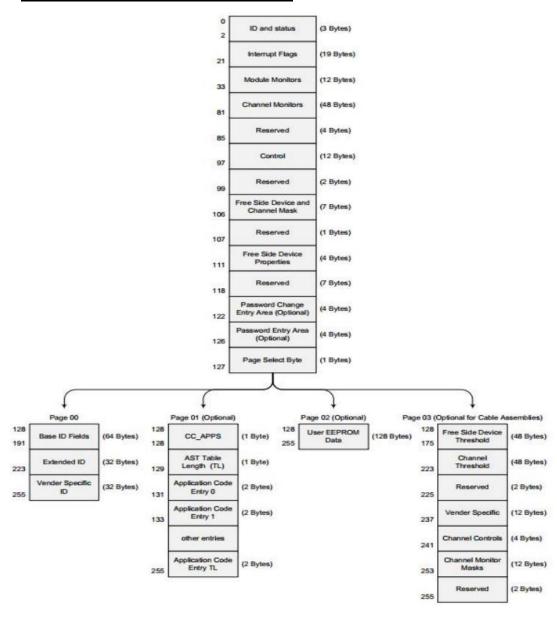


Figure 5.1 QSFP28 Memory Map

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5.2 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Table 5.2 Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	±3	deg.C
Internally Measured Transceiver Supply Voltage	±5	%
Measured Tx Bias Current	±10	%
Measured Tx Output Power	±3	dB
Measured Rx Received Average Optical Power	±3	dB

6. Pin Assignment and Pin Description

QSFP28 transceiver pad layout, host PCB QSFP28 pinout, and PIN descriptions are as follows:

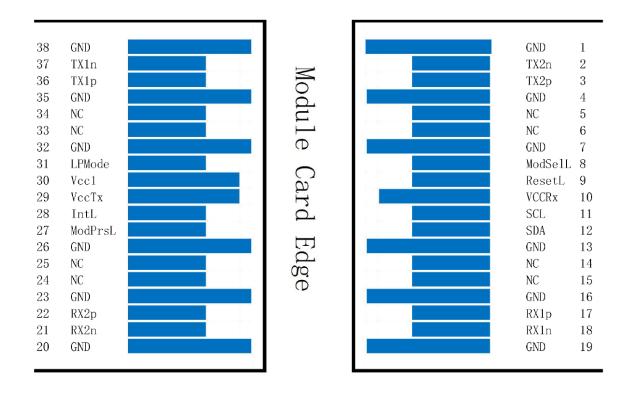


Figure 6.1 QSFP28 Transceiver Electrical Pad layout

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Table 6.1 Pin Description

1	Pin	Logic	Symbol	Description	Plug Sequence	Notes
3	1		GND	Ground	1	1
Signature	2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
5 CML-I Tx4n Transmitter Inverted Data Input 3 3 6 CML-I Tx4p Transmitter Non-Inverted Data Input 3 3 7 GND Ground 1 1 1 8 LVTTL-I ResetL Module Select 3 3 9 LVTTL-I ResetL Module Reset 3 3 10 Vcc Rx +3.3V Power Supply Receiver 2 2 2 11 LVCMOS-I/O SCL 2-wire serial interface clock 3 3 12 LVCMOS-I/O SCL 2-wire serial interface clock 3 3 13 GND Ground 1 1 1 14 CML-O Rx3p Receiver Inverted Data Output 3 3 3 16 GNL-O Rx1p Receiver Inverted Data Output 3 3 3 1 1 1 1 1 1 1 1 1 1 1 1	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
6 CML-I Tx4p Transmitter Non-Inverted Data Input 3 3 7 GND Ground 1 1 8 LVTTL-I ModselL Module Select 3 9 LVTTL-I Resett. Module Reset 3 10 Vcc Rx +3.3V Power Supply Receiver 2 2 11 LVCMOS-I/O SCL 2-wire serial interface clock 3 12 LVCMOS-I/O SDA 2-wire serial interface data 3 13 GND Ground 1 1 1 14 CML-O Rx3p Receiver Non-Inverted Data Output 3 3 3 15 CML-O Rx3p Receiver Inverted Data Output 3 3 3 3 16 GND-O Rx1p Receiver Inverted Data Output 3 3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4		GND	Ground	1	1
7 GND Ground 1 1 1 8 LVTTL-I Module Select 3 3 9 LVTTL-I ResetL Module Reset 3 10 VCc Rx +3.3V Power Supply Receiver 2 2 11 LVCMOS-I/O SCL 2-wire serial interface clock 3 12 LVCMOS-I/O SDA 2-wire serial interface data 3 13 GND Ground 1 1 1 14 CML-O Rx3p Receiver Non-Inverted Data Output 3 3 15 CML-O Rx3p Receiver Inverted Data Output 3 3 16 GND Ground 1 1 1 17 CML-O Rx1p Receiver Inverted Data Output 3 3 18 CML-O Rx1p Receiver Inverted Data Output 3 3 19 GND Ground 1 1 1 20 CML-O Rx2p	5	CML-I	Tx4n	Transmitter Inverted Data Input	3	3
8 LVTTL-I Module Select 3 9 LVTTL-I ResetL Module Reset 3 10 Vcc Rx +3.3V Power Supply Receiver 2 2 11 LVCMOS-I/O SCL 2-wire serial interface clock 3 12 LVCMOS-I/O SDA 2-wire serial interface data 3 13 GND Ground 1 1 1 14 CML-O Rx3p Receiver Non-Inverted Data Output 3 3 3 15 CML-O Rx3n Receiver Inverted Data Output 3 3 3 16 GND Ground 1	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	3
Second	7		GND	Ground	1	1
10	8	LVTTL-I	ModselL	Module Select	3	
11	9	LVTTL-I	ResetL	Module Reset	3	
12	10		Vcc Rx	+3.3V Power Supply Receiver	2	2
13	11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
14 CML-O Rx3p Receiver Non-Inverted Data Output 3 3 15 CML-O Rx3n Receiver Inverted Data Output 3 3 16 GND Ground 1 1 1 17 CML-O Rx1p Receiver Non-Inverted Data Output 3 3 18 CML-O Rx1n Receiver Inverted Data Output 3 1 1 1 19 GND Ground 1	12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
15	13		GND	Ground	1	1
1	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	3
17 CML-O Rx1p Receiver Non-Inverted Data Output 3 18 CML-O Rx1n Receiver Inverted Data Output 3 19 GND Ground 1 1 20 GND Ground 1 1 21 CML-O Rx2n Receiver Inverted Data Output 3 22 CML-O Rx2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 1 24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I </td <td>15</td> <td>CML-O</td> <td>Rx3n</td> <td>Receiver Inverted Data Output</td> <td>3</td> <td>3</td>	15	CML-O	Rx3n	Receiver Inverted Data Output	3	3
18 CML-O Rx1n Receiver Inverted Data Output 3 19 GND Ground 1 1 20 GND Ground 1 1 21 CML-O Rx2n Receiver Inverted Data Output 3 22 CML-O Rx2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 1 24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 1 27 LVTTL-O ModPrsL Module Present 3 3 3 28 LVTTL-O IntL Interrupt 3 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 2 30 Vcc1 +3.3V Power supply 2 2 2 31 LVTL-I LPMode L	16		GND	Ground	1	1
19	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
CML-O	18	CML-O	Rx1n	Receiver Inverted Data Output	3	
21 CML-O Rx2n Receiver Inverted Data Output 3 22 CML-O Rx2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 1 24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 1 27 LVTTL-O ModPrsL Module Present 3 3 3 28 LVTTL-O IntL Interrupt 3 3 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 2 30 Vcc1 +3.3V Power supply 2 2 2 31 LVTTL-I LPMode Low Power Mode 3 3 32 GND Ground 1 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3	19		GND	Ground	1	1
22 CML-O Rx2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 1 24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Non-Inverted Data Input 3 3 36 CML-I Tx1p Transmitter Non-Inverted Data Input <t< td=""><td>20</td><td></td><td>GND</td><td>Ground</td><td>1</td><td>1</td></t<>	20		GND	Ground	1	1
23 GND Ground 1 1 24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3 <td>21</td> <td>CML-O</td> <td>Rx2n</td> <td>Receiver Inverted Data Output</td> <td>3</td> <td></td>	21	CML-O	Rx2n	Receiver Inverted Data Output	3	
24 CML-O Rx4n Receiver Inverted Data Output 3 3 25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Non-Inverted Data Input 3 3 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
25 CML-O Rx4p Receiver Non-Inverted Data Output 3 3 26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 3 37 CML-I Tx1n Transmitter Inverted Data Input 3 3	23		GND	Ground	1	1
26 GND Ground 1 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3	24	CML-O	Rx4n	Receiver Inverted Data Output	3	3
27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 3 37 CML-I Tx1n Transmitter Inverted Data Input 3 3	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	3
28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3	26		GND	Ground	1	1
29 Vcc Tx +3.3V Power supply transmitter 2 2 30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 3 37 CML-I Tx1n Transmitter Inverted Data Input 3 3	27	LVTTL-O	ModPrsL	Module Present	3	
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30 Vcc1 +3.3V Power supply 2 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3	20		Vcc Tv	+3.3\/ Power supply transmitter	2	2
31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3						
32 GND Ground 1 1 33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3		IVTTI -I				
33 CML-I Tx3p Transmitter Non-Inverted Data Input 3 3 34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3		LVIIL-I			-	1
34 CML-I Tx3n Transmitter Inverted Data Input 3 3 35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3		CML-I			-	-
35 GND Ground 1 1 36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3				·		
36 CML-I Tx1p Transmitter Non-Inverted Data Input 3 37 CML-I Tx1n Transmitter Inverted Data Input 3		OIVIL-I		·		
37 CML-I Tx1n Transmitter Inverted Data Input 3		CMI -I				
	38	OIVIL-I	GND	Ground	1	1

Note:

- [1] GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
- [2] Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.
- [3] Not used.



7. Package Dimensions

Figure 7.1 shows the package dimensions of the module. The module is designed to be complaint with QSFP28 MSA specification. Package dimensions are specified in SFF-8661.

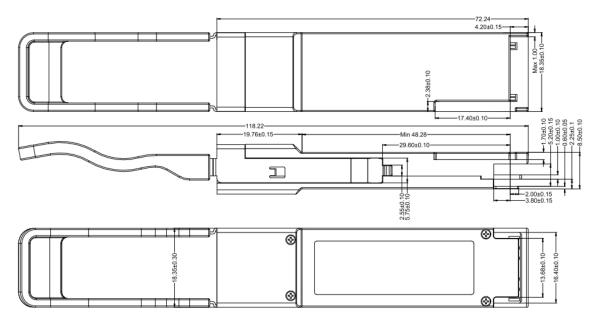


Figure 7.1 Package Dimensions

8. Laser safety and Electromagnetic Compatibility

8.1 Laser safety

All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825-1 & IEC60825-2 standards. They must be operated under specified operating conditions.

8.2 Electromagnetic Compatibility

All transceivers are designed to meet FCC Class B limits.

9. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E
L-QSFP28-ER2-40	0°C to + 70°C	40km	SMF	EML	APD

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